

PATENT

Serial No. 10/523,666

Amendment in Reply to Final Office Action mailed on November 20, 2006

IN THE SPECIFICATION

Please amend the specification as follows:

Replace the paragraph on page 7, between lines 23-32 of the specification with the following:

Fig. 1 shows the principle structure of the control unit controlling a threshold voltage of a circuit unit. The module comprises a circuit unit 2 for providing different threshold voltages V_{t1} through line 4, V_{t2} through line 6, and V_{tn} through line 8, and a reference voltage V_{trf} through line 10 to the ΔV_t monitor 12. The monitor 12 creates the average threshold voltage value of the circuit unit 2. The monitor 12 outputs a dc reference V_R and the ~~the~~ averaged threshold voltage difference ΔV_t through line 14 and receives the reference voltage V_R through ~~line 16~~ line 10. The reference voltage V_R is also supplied to the plus terminal of an amplifier 18. The amplifier 18 receives the average threshold voltage difference $\Delta V_t + V_R$ on its plus terminal and the reference voltage V_R on its minus terminal. The amplifier 18 outputs the biasing voltage V_b through line 20 to the circuit unit 2.

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Replace the paragraph on page 12, between lines 3-19 of the specification with the following:

Fig. 7 shows in principle an extension of the Fig. 6. In each branch of the current ~~mirror 66~~ mirror 60 is the same number of transistors connected in parallel between the current ~~mirror 66~~ mirror 60 and ground. The branch of the so-called circuit unit comprises three transistors 68, 70, and 72. The drain contacts are connected in parallel, the gate contacts are connected in parallel and the drain-source contacts are connected in parallel. The ~~drain~~ source contacts are connected to ground. The drain contacts are connected in parallel to the current mirror 60. The gate contacts are connected to the terminal 80. In principle the same is done with the right branch of the current ~~mirror 66~~ mirror 60. The right branch comprises three transistors 74, 76, 78. The ~~drain-source~~ contacts are connected in parallel to ground. The gate contacts are connected in parallel to the terminal 82. The drain contacts are connected in parallel to the current ~~mirror 66~~ mirror 60. The same number of transistors has to be used in both branches of the circuit or an equivalently wide transistor in one of the branches in order to have $I_1 \approx I_2$, getting almost the same expression of (6)

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Replace the paragraph on page 15, between lines 14-22 of the specification with the following:

Fig. 14 shows a layout for power supply and bulk line routing. The layout comprises a power supply line 174, a ground line 176, standard cells 178, 180, 182 and a bulk line 184. The standard cells 178, 180, 182 consist of an arrangement of P-MOSFETs and or N-MOSFETs. One has to exercise care for the layout as biasing the bulk independently from the source can give origin to latch-up problems, or to induced noise in the bulk line. We propose a closed-loop scheme for power supply and bulk biasing. ~~Fig. 16~~ Fig. 14 shows details for routing the power supply and bulk line for the particular case of NMOS V_t control. Note that there is a choice in making contacts to the well. This can be done for every cell or every N cells.